2A, 4.5V-20V Input，500kHz Synchronous Step-Down Converter

■ General Description

LN8120 is a fully integrated, high– efficiency 2A synchronous rectified step-down converter. The LN8120 operates at high efficiency over a wide output current load range.

This device offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load.

The LN8120 requires a minimum number of readily available standard external components and is available in an 6-pin SOT23 ROHS compliant package.

■ Applications

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Wireless and DSL Modems
- Notebook Computer

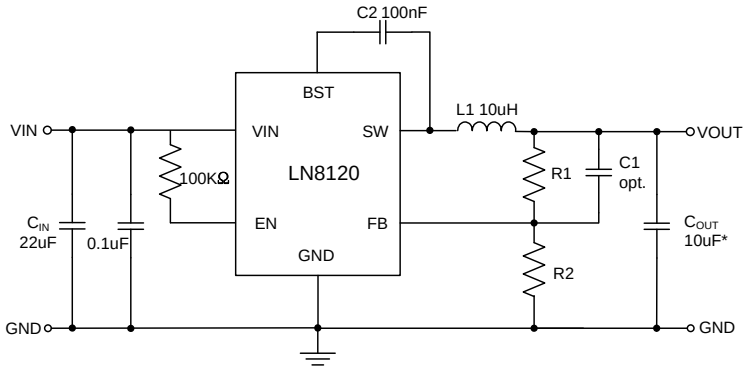
■ Features

- High Efficiency: Up to 96%
- 500KHz Frequency Operation
- 2A Output Current
- No Schottky Diode Required
- 4.5V to 20V Input Voltage Range
- 0.6V Reference
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Integrated internal compensation
- Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection with Hiccup-Mode
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Available in SOT23-6 Package
- -40°C to +85°C Temperature Range

■ Package

- SOT-23-6L

■ Typical Application Circuit



Note: 1. Avoid short between BST and SW

2. 200 kΩ > R1 > 150 kΩ; if R1 is less than 150 kΩ, be sure to use 22uF or greater

3. Input capacitance recommended use of a 22uF electrolytic capacitor.

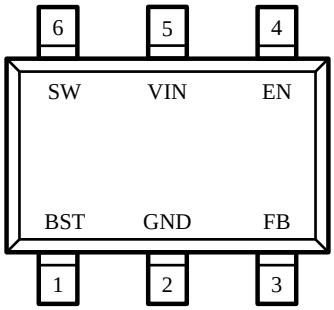
4. If use larger output capacitor (Eg. 220uF), please contact salesperson.

■ Ordering Information

LN8120P①②③

Designator	Symbol	Description
①	6	External feedback, Feedback Voltage 0.6V
		External feedback, Feedback Voltage 0.8V
②	M	Package Type :SOT-23-6L
③	R	Embossed Tape : Standard Feed
	L	Embossed Tape : Reverse Feed

■ Pin Configuration

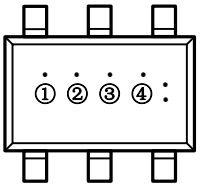


SOT-23-6L
(TOP VIEW)

■ Pin Assignment

Pin Number SOT-23-6L	Pin Name	Function
1	BST	Bootstrap pin. Connect a 100nF capacitor from this pin to SW
2	GND	Ground
3	FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set VOUT
4	EN	Enable pin for the IC. Drive this pin high to enable the part, low to disable.
5	IN	Supply Voltage. Bypass with a 22μF ceramic capacitor to GND
6	SW	Inductor Connection. Connect an inductor Between SW and the regulator output.

■ Marking Rule



SOT-23-6L
(TOP VIEW)

① Represents the product name

Symbol	Product Name
7	LN8120P***

② Represents the feedback voltage

Symbol	Description
A	Feedback Voltage 0.6V
	Feedback Voltage 0.8V

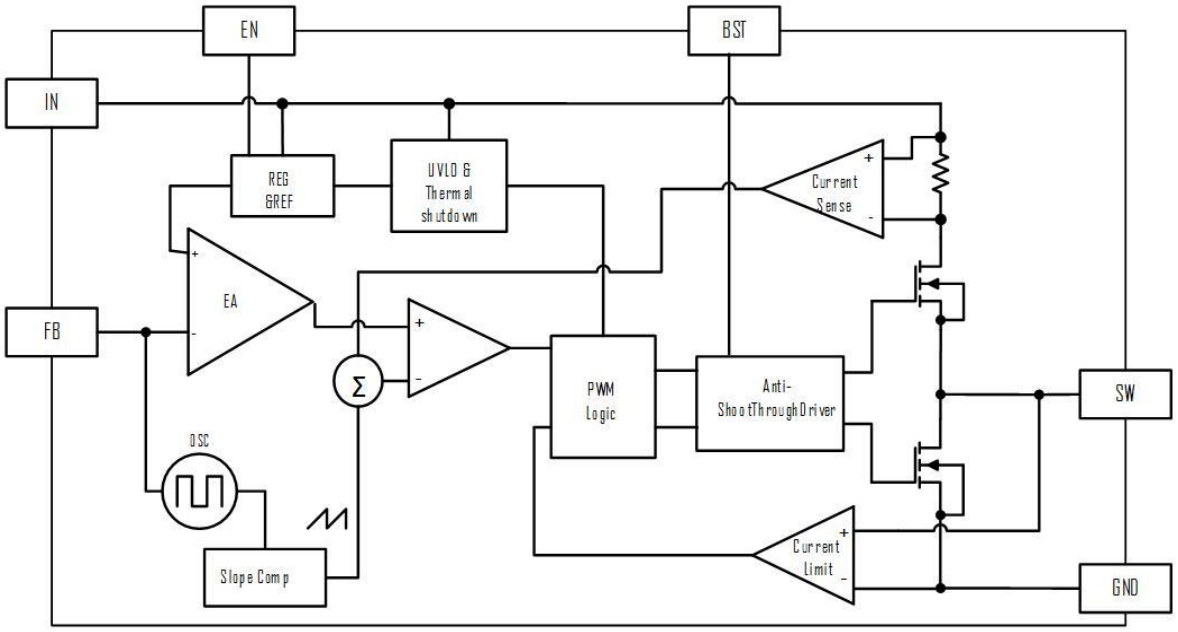
③ Represents the packaging information

Symbol	Package
6	SOT23-6L

④ Represents the assembly lot No.

0-9，A-Z; 0-9，A-Z mirror writing，repeated（G，I，J，O，Q，W exception）

■ Function Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Maximum Rating		Unit
Input Voltage	V_{IN}	V_{SS}-0.3～V_{SS}+21		V
	$V_{ON/OFF}$	V_{SS}-0.3～V_{IN}+0.3		
SW Voltage		V_{SS}-0.3～V_{IN}+0.3		
BST Voltage		V_{SS}-0.3～SW+6		
FB Voltage		V_{SS}-0.3～V_{SS}+6		
Power Dissipation	P_D	SOT-23-6L	600	mW
Operating Ambient Temperature	Topr	-40～+85		°C
Storage Temperature	Tstg	-40～+125		
ESD HBM (Human Body Mode)		2		KV
ESD MM (Machine Mode)		200		V

Caution: The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

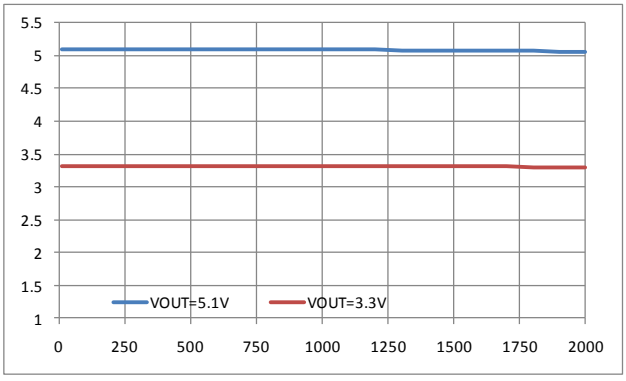
■ Electrical Characteristics

Note：VIN = 12V, VOUT = 3.3V, unless otherwise specified. Typical values are at TA = 25℃)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	V_{IN}		4.5		20	V
Supply Current	I_{SS1}	V_{EN}=2V，V_{FB}=0.85V		380		μA
Supply Current	I_Q	V_{IN}=12V，V_{OUT}=3.3V No load		410		uA
Supply Shutdown Current	I_{SS2}			1		μA
FB Voltage	V_{FB}	T_A=25°C，4.5V≤V_{IN}≤18V	0.588	0.6	0.612	V
Switching Frequency	F_{OSC}			500		kHz
Maximum Duty Cycle	DMAX			96		%
FB Hiccup Threshold	V_{FB-HT}			0.15		V
High Side Switch On Resistance	R_{DSON_H}			90		mΩ
Low Side Switch On Resistance	R_{DSON_L}			70		mΩ
High Side Current Limit	I_{LIM}			3		A
EN Rising Threshold	V_{CEH}				2	V
EN Falling Threshold	V_{CEL}		0.5			V
EN Input Current	I_{EN}	VEN=2V		1		uA
Thermal Shutdown	T_{SHD}	Rising, Hysteresis =40°C		150		°C

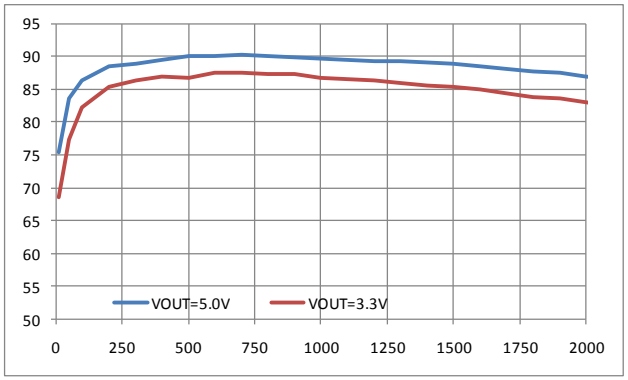
■ Typical Performance Characteristics

Load Regulation



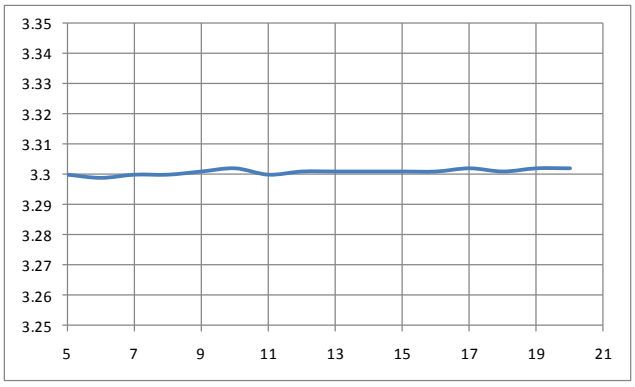
Load Current (mA)

Efficiency vs. Load Current



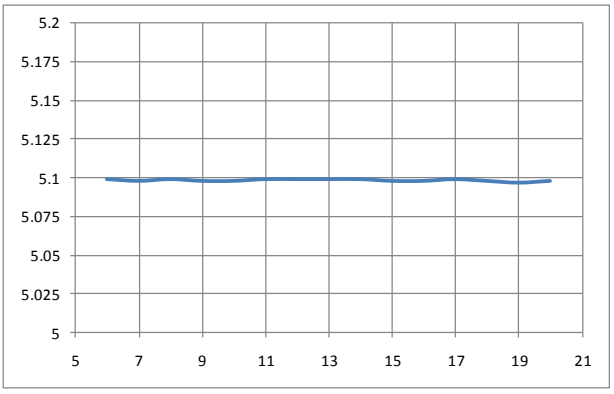
Load Current (mA)

Line Regulation



Input Voltage (V)

Line Regulation



Input Voltage (V)

VOUT=3.3V, 1.5A -> 0.2A ->1.5A load jump

■ Functional Description

Internal Regulator

The LN8120 is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at 500K operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

EA Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (VFB) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current.The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Enable

EN is a digital control pin that turns the LN8120 on and off. Drive EN High to turn on the regulator, drive it Low to turn it off. An internal 1MΩ resistor from EN pin to GND allows EN to float to shut down the chip. Connecting the EN pin through a pull up resistor or shorted EN to IN will automatically turn on the chip whenever plug in IN.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to 1 ms.

Over-Temperature Protection

Thermal protection disables the output when the junction temperature rises to approximately 150°C, allowing the device to cool down. When the junction temperature cools to approximately 120°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Over-Current-Protection and Hiccup

The LN8120 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the LN8120 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The LN8120 exits the hiccup mode once the over current condition is removed.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

■ Application Information

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 100kΩ for optimal transient response.R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1}$$

Inductor Selection

A 4.7μH to 22μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

ere: VFB =0.6V typically (the internal reference voltage)

Resistors R2 has to be between 1kOhm to 20KOhm and thus R1 is calculated by following equation.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22μF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.

Output Capacitor Selection

The output capacitor (COUT) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{OSC} \times C_{OUT}})$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{V_{IN} \times {f_{OSC}}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{OSC} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The LN8120 can be optimized for a wide range of capacitance and ESR values.

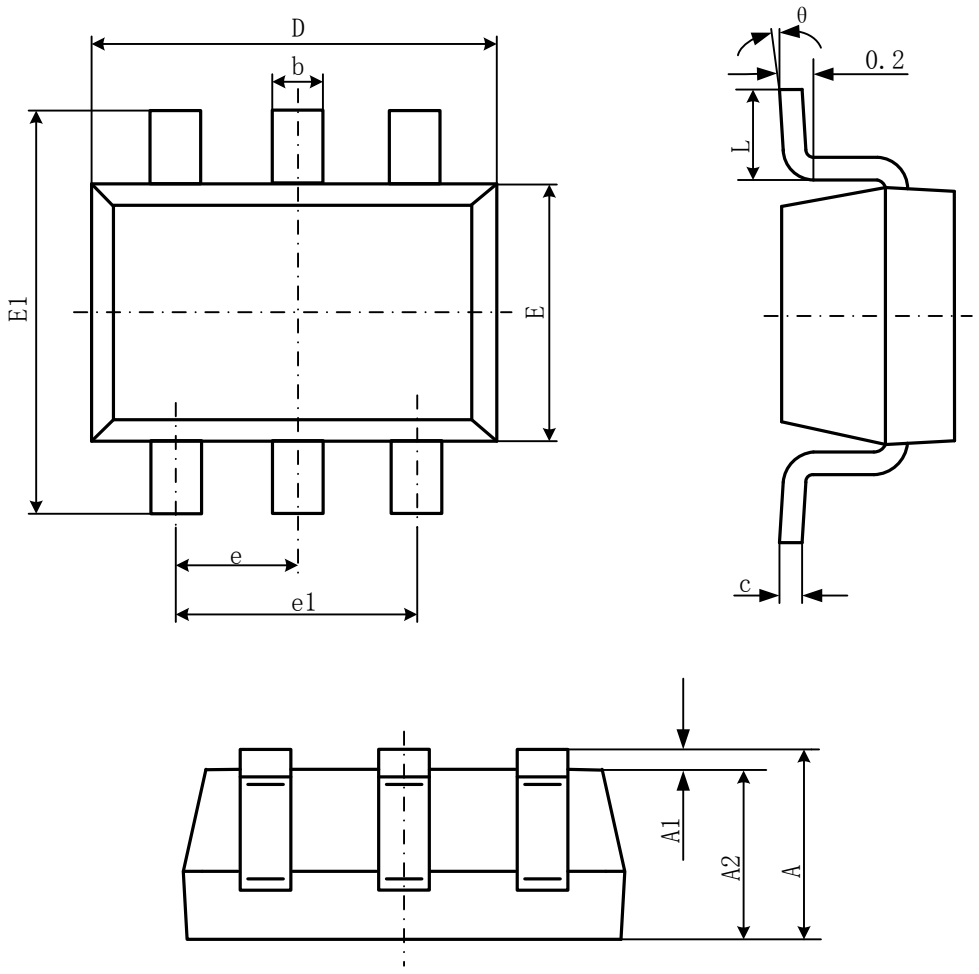
■ Application Information

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 3 for reference.

- Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
- Bypass ceramic capacitors are suggested to be put close to the VIN Pin.
- Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- V_{OUT}, SW away from sensitive analog areas such as FB.
- Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.
- An example of 2-layer PCB layout is shown in Figure 3 for reference.

■ Package Information

- **SOT-23-6L**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°